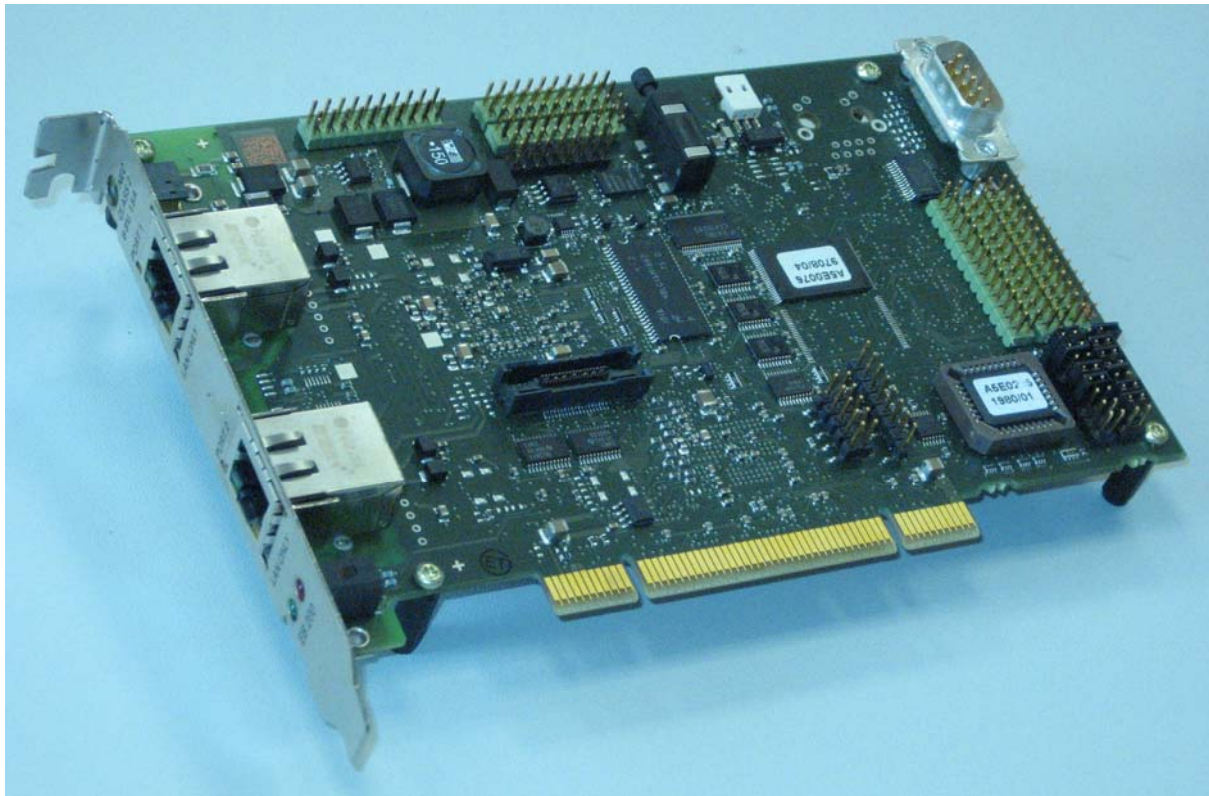




EB 200

Evaluation Board ERTEC 200

Manual



Disclaimer of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly. Necessary corrections are included in subsequent editions. Suggestions for improvement are welcomed.

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Preface

Contents of this Manual

- ❑ Detailed description of the individual function groups of the EB 200
- ❑ Connector pin assignment and jumper assignment

Target Audience of this Manual

This manual is intended for hardware developers who want to use the ERTEC 200 for new products. Experience working with processors and designing embedded systems and knowledge of Ethernet are required for this.

The manual serves as a reference for software developers. Sections 7 and 8 describe the jumper settings and connectors that are required for software tests (e.g., debugging, terminal outputs, etc.).

Structure of this Manual

This manual describes the ERTEC 200 evaluation board. The manual is structured as follows:

- Section 1 Introduction
- Section 2 Hardware Structure of the EB 200
- Section 3 Memory Distribution of the EB 200.
- Section 4 Operating Modes of the EB 200
- Section 5 JTAG Interface of the EB 200
- Section 6 Settings of the EB 200
- Section 7 Connectors of the EB 200
- Section 8 Jumpers of the EB 200
- Section 9 Mechanical Structure of the EB 200
- Section 10 List of Terms and References

When working with modules, always take precautionary measures against electrostatic charge (ESD – Electrostatic Sensitive Devices).

For module handling and installation, refer to /3/.

This manual will be updated as required. You can find the current version of the manual on the Internet at <http://www.siemens.com/comdec>.

Guide

To help you quickly find the information you need, this manual contains the following aids:

- A complete table of contents as well as a list of all figures and tables in the manual are provided at the beginning of the manual.
- A glossary containing definitions of important terms used in the manual is located following the appendices.
- References to other documents are indicated by the document reference number enclosed in slashes (/No./). The complete title of the document can be obtained from the list of references at the end of the manual.

Additional Support

If you have questions regarding use of the described block that are not addressed in the documentation, please contact your Siemens representative.

Please send your written questions, comments, and suggestions regarding the manual to the hotline via the e-mail address indicated above.

In addition, you can receive general information, current product information, FAQs, and downloads pertaining to your application on the Internet at:

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1 Introduction

This manual describes the procedure for using the ERTEC 200 for HW development of a PROFINET IO device and the properties of the EB 200 evaluation board.

The intended use of the EB 200 evaluation board is as follows:

- It serves as a template for development of your own PROFINET IO device hardware.
- It supports development and testing of your own PROFINET IO device application software.
- It enables testing of your hardware on a supplementary board together with the EB 200, where applicable.

1.1 Procedure when Using ERTEC 200 to Develop Your Own PROFINET IO Device

The "DK-ERTEC200 PN IO" CD contains two circuit diagrams:

1. Circuit diagram of the EB 200 [EB200 circuit diagrams.pdf](#)
2. Minimum configuration for a PROFINET IO device [EB200 AN001 minimal circuit configuration.pdf](#)

If you are using the recommended minimum configuration for a PROFINET IO device, no changes (or only minor changes) have to be made in the board support package (BSP) for your additionally required hardware. The board support package adapts the operating system to the hardware, see /3/.

Procedure

You can use ERTEC 200 to develop your own hardware in one of two ways:

- By using a test board on the EB 200 to adapt and test your application circuit
- By using ERTEC 200 directly to develop and test your complete target hardware

Note the following boundary conditions for hardware development:

Minimum Memory Capacity

Memory Type	Minimum	Recommended
Flash AMD29DL323GB-90EI/T AMD	4 Mbytes	4 Mbytes
SDRAM HYP39S25616DT-7.5 Infineon	32 Mbytes	64 Mbytes

Debug Interfaces for Commissioning and Testing

Always make provision for connectors on your hardware to the JTAG interface and, if possible, to a serial interface (UART1) of the ERTEC 200 in order to facilitate commissioning.

1.2 Structure of the EB 200

The EB 200 is implemented in the form of a PCI card. The PCI interface is used only for module tests. In standard configuration the EB 200 is operated as a stand-alone module. The EB 200 is supplied by means of an external plug-in power supply (part of the development kit). For debugging the Amontec JTAG debugger including usb cable (both also part of the development kit) can be plugged onto the EB200 as shown in the following picture.



1.3 Features of the EB 200

In addition to the ERTEC 200 with its integrated function groups, the following elements are available on the EB 200:

- PC front panel element with
 - 2 RJ45 sockets with integrated magnetics
 - 2 LEDs **Link** and **Activity** per RJ45 socket → Optional LED display **Speed** and **Duplex**
 - 2 LEDs for additional status indicators
 - External DC power supply in stand-alone mode
- Flash memory 4 Mbytes
- Flash memory 512 Kbytes, socketed PLCC32
- SDRAM 64 Mbytes
- SRAM 8 Mbytes
- SPI Data Flash and EPROM
- Debug and trace interface for ARM946ES-μP
- RS232 interface for booting, debugging, and monitoring
- Configuration and boot modes can be set via jumpers
- Various operating modes of the EB 200 can be set via jumpers
- Various connectors for external wiring

1.4 Block Diagram of the EB 200

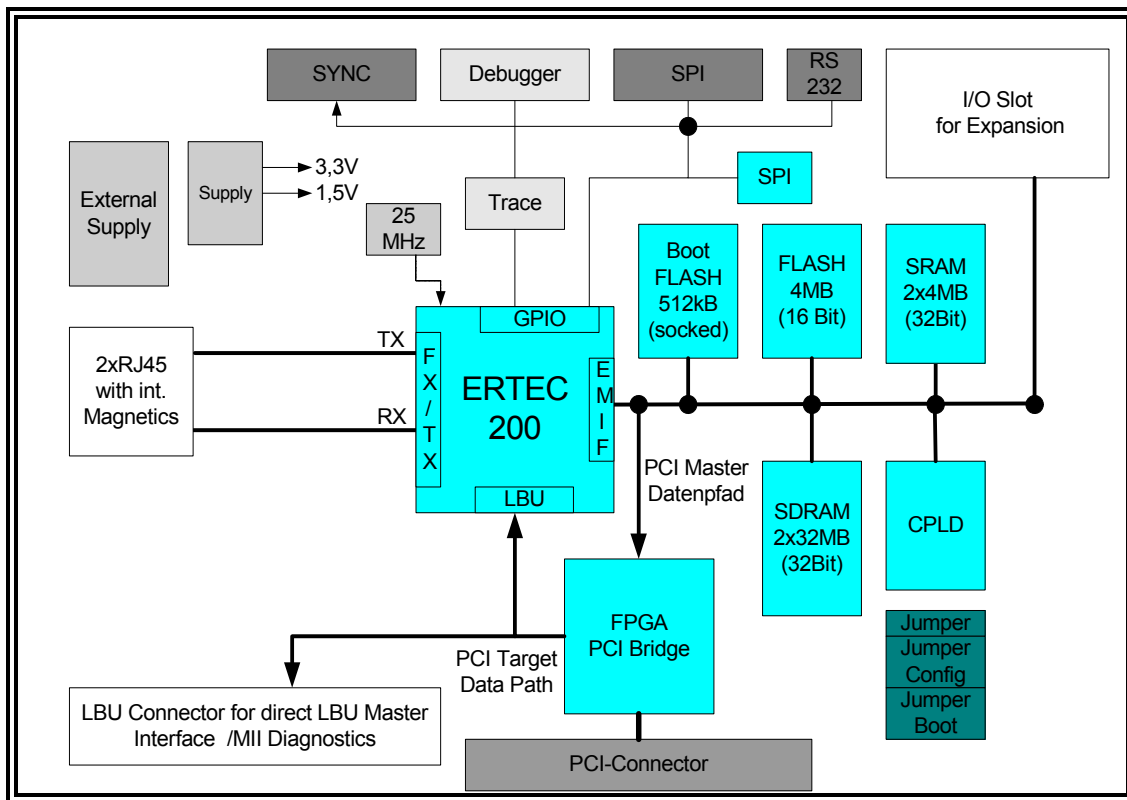


Figure 1: Block Diagram of the EB 200

Note: On the evaluation board EB200 (hardware release ES35 and newer), that is included in the development kit V3.2.0 and newer, the following components are no more used and no more assembled:

- NAND-Flash
- SMSC-LAN91C111 Ethernet Chip
- RJ45-female connector.

The boards are fully compatible to the prior version ES34, there are no limitations on functionality for PROFINET.

2 Hardware Structure of the EB 200

2.1 ERTEC 200

2.1.1 Function Overview

Refer to documents /1/ and /2/ for a detailed function description of the ERTEC 200.

In this manual, only the main components are described briefly and represented in a block diagram.

The following four AHB masters are integrated in the ERTEC 200:

- ARM946E-S with trace/debug port and high-performance interrupt controllers
- IRT switch with 64 Kbytes of K-RAM for real-time Ethernet communication
- External host processor on the LBU interface
- Single channel DMA controller

The following I/O blocks are available to the masters:

- External memory interface (EMIF) with SDRAM and SRAM controller
- Two Ethernet interfaces with integrated MII PHYs
- I/O via APB bridge
 - 45-bit GPIO
 - UART
 - SPI
 - 3 timers
 - F-timer
 - Watchdog
 - Boot ROM
 - System function register

The multi-layer AHB bus system enables a largely independent operation of the masters. An internal arbitration logic prevents access conflicts if multiple masters want to access the same I/O block. The function groups of the ERTEC 200 are shown in the following block diagram:

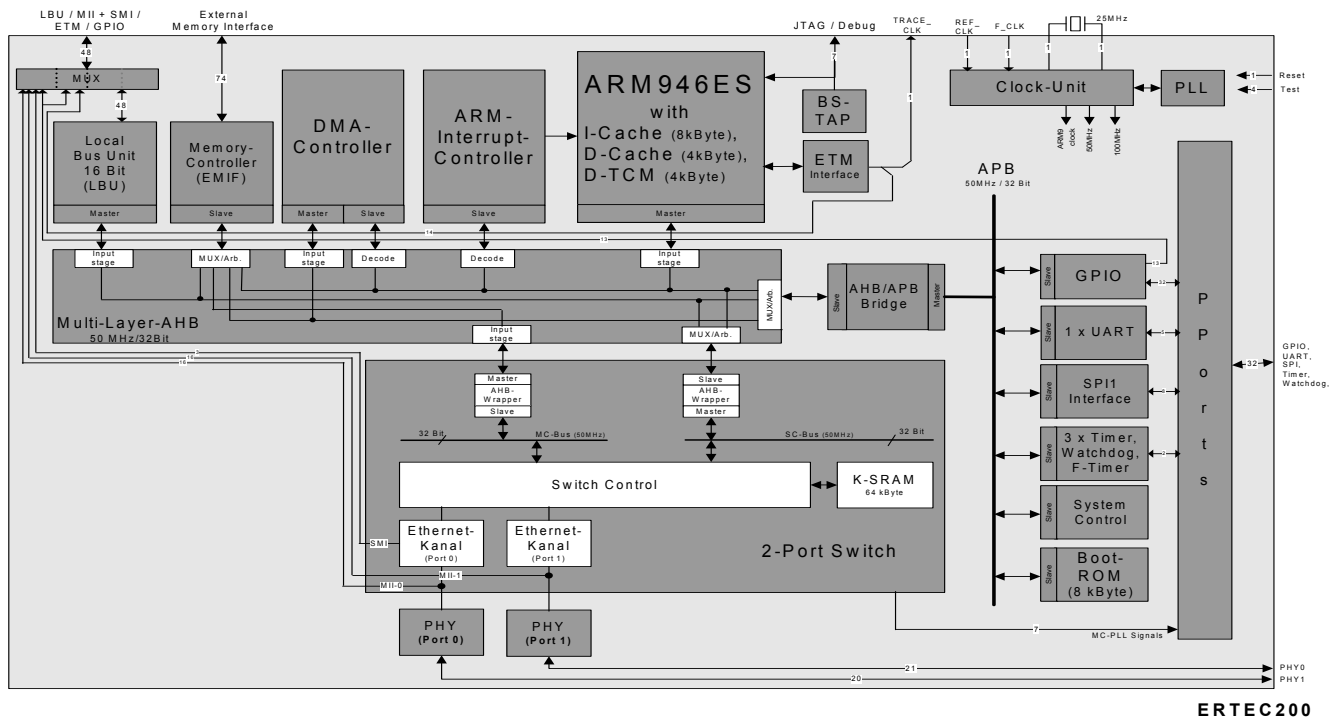


Figure 2: ERTEC 200 Block Diagram

2.1.2 Operating Modes of the EB 200

Various configurations on the EB 200 can be set by means of jumpers X10.9/10 to X11.3/4. These jumpers are described in Section 8. The following configuration settings are possible on the ERTEC 200.

CONFIG[6] X11 3/4	CONFIG[5] X11 1/2	CONFIG[4] X10 15/16	CONFIG[3] X10 13/14	CONFIG[2] X10 11/12	CONFIG[1] X10 9/10	Meaning
-	-	-	-	-	1	REF_CLK tristate
-	-	-	-	-	0	REF_CLK output (25 MHz)
-	1	-	-	0	-	LBU = On → LBU-CFG: LBU_WR_N has read/write control
-	0	-	-	0	-	LBU = On → LBU-CFG: Separate read and write line
1	-	-	-	0	-	LBU = On → LBU_POL_RDY: LBU_RDY_N is high-active
0	-	-	-	0	-	LBU = On → LBU_POL_RDY: LBU_RDY_N is low-active
0	1	-	-	1	-	LBU = Off → GPIO44-32 = On int. PHYs = On, ext. MII = PHY debugging, ETM9 = Off
1	0	-	-	1	-	LBU = Off → GPIO44-32 = On int. PHYs = On, ext. MII = Off, ETM9 = On
1	1	-	-	1	-	LBU = Off → GPIO44-32 = On int. PHYs = Off, ext. MII = On, ETM9 = Off
-	-	0	0	-	-	ARM clock 50 MHz
-	-	0	1	-	-	ARM clock 100 MHz
-	-	1	0	-	-	ARM clock 150 MHz
-	-	1	1	-	-	Reserved

- LBU mode: CONFIG[2] = 0
The LBU interface is active for access of a host processor system to internal components of the ERTEC 200. The internal PHYs are used in this operating mode. Debugging of internal PHYs and diagnostics via the trace interface are not possible in this mode.
- MII diagnostics: CONFIG[2] = 1; CONFIG[5] = 1; CONFIG[6] = 0;
Diagnostics of the signals between internal PHYs and IRT switch is possible in this mode. The GPIO[44:32] is also available.
- Trace mode: CONFIG[2] = 1; CONFIG[5] = 0; CONFIG[6] = 1;
The trace port and the GPIO[44:32] are available to the user in this mode.

X11 5/6		Meaning
SPI_CONFIG	1	SPI Boot Mode 1 (EEPROM)
	0	SPI Boot Mode 2 (Flash)

X11					Open = 1 For = 0
Pin 15,16	Pin 13,14	Pin 11,12	Pin 9,10	Pin 7,8	
SYS_Config[4]	SYS_Config[3]	SYS_Config[2]	SYS_Config[1]	SYS_Config[0]	Meaning
-	-	-	0	0	LBU Mode LBU On internal PHY's = on external MII = off ETM-Trace = off GPIO 32-44 = off
-	-	-	1	0	PHY debugging LBU = Off Internal PHYs = On External MII = PHY debugging ETM trace = Off GPIO 32-44 = On
-	-	-	0	1	Trace mode LBU = Off Internal PHYs = On External MII = Off ETM trace = On GPIO 32-44 = On
-	-	-	1	1	PCI-LBU Bridge Mode
-	-	0	-	-	RS232 = Off
-	-	1	-	-	RS232 = On
-	0	-	-	-	RS485 = Off
-	1	-	-	-	RS485 = On
0	-	-	-	-	Disable GPIO interrupts
1	-	-	-	-	Enable GPIO interrupts

Table 1: Selection of Operating Modes and System Functions for EB 200

2.1.3 Boot Modes of the EB 200

Various boot modes on the EB 200 can be set by means of jumpers X10.1/2 to X10.7/8.

Additional jumper settings on connector X11 5/6 are necessary in SPI boot mode. These jumpers are described in Sections 8.1 and 8.2. The following download modes are supported:

BOOT[3] X10 7/8	BOOT[2] X10 5/6	BOOT[1] X10 3/4	BOOT[0] X10 1/2	BOOTING OF
0	0	0	0	External ROM with 8-bit data width
0	0	0	1	External ROM with 16-bit data width
0	0	1	0	Reserved
1	0	0	0	Fast External ROM with 8-bit data width
1	0	0	1	Fast External ROM with 16-bit data width
1	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	SPI1
0	1	1	0	UART
0	1	1	1	LBU
1	0	1	1	Reserved

Table 2: Boot Mode Selection for EB 200

For all jumpers: 0 = jumper inserted, 1 = jumper not inserted

2.1.4 ERTEC 200 Processor and I/O

The ARM946E-S processor with interrupt controller is integrated in the ERTEC 200. The processor and various standard I/O are available to users for their applications. These include the following function groups:

- ARM946E-S processors with
 - 50/100/150 MHz operating frequency that can be set via jumpers (see Operating Modes 2.1.2)
 - 8 Kbytes of instruction cache
 - 4 Kbytes of data cache
 - 4 Kbytes of data TCM
 - JTAG interface for debug interface
- Interrupt controller for asynchronous events (16 IRQ and 8 FIQ inputs)
- SDRAM controller 50 MHz/max. 128 Mbytes of address space (16/32-bit data width can be assigned)
- SRAM controller, up to 4 x 16 Mbytes (8/16/32-bit data width and timing can be assigned separately for all 4 areas)
- Watchdog timer unit for monitoring module functions
- Timer unit for generating periodic trigger pulses
- F-timer for fail-safe applications
- GPIO ports for activating LEDs, etc.
- SPI interface for connecting serial EEPROM/Flash
- UART

2.1.5 PCI Interface

A PCI bridge enabling connection to a PCI bus is integrated in the ERTEC 200 by means of an FPGA. However, the PCI interface is used only for the function test of the EB 200.

2.1.6 IRT switch

The IRT switch provides the required function for PROFINET IO. It contains the following functions:

- Configuration register for IRT switch
- 64 Kbytes of K-RAM for RT and IRT communication

The IRT switch functions are described in document /3/.

2.1.7 Interrupt System of the EB 200

The EB 200 has two interrupt controller units that can only be operated by the ARM946E-S.

- IRQ controller unit with 16 inputs for low-priority interrupts
- FIQ controller unit with 8 inputs for high-priority interrupts

The IRQ/FIQ interrupt sources are listed in the tables below.

INTERRUPT #	BLOCK SOURCE	SIGNAL	DEFAULT	COMMENT
0	Timer0	TIM_INT0	Rising edge	Timer 0
1	Timer1	TIM_INT1	Rising edge	Timer 1
3:2	GPIO	GPIO1/0	Assignable	ERTEC 200 pins GPIO_IO[1:0]
5:4	GPIO	GPIO31/30	Assignable	ERTEC 200 pins GPIO_IO[31:30]
6	Timer2	TIM_INT2	Rising edge	Timer 2
7	--	--	--	Reserved
8	UART	UARTINTR	High level	Group interrupt UART
9	PHY0/1	P1/2_INTERP	Rising edge	Interrupt from PHY1/2
10	SPI1	SSPINTR	Rising edge	SPI1 group interrupt
11	SPI1	SSPRORINTR	Rising edge	SPI Receive overrun interrupt
12	IRT switch control	IRQ0_SP	Rising edge	High-priority IRTE interrupt
13	IRT switch control	IRQ1_SP	Rising edge	Low-priority IRTE interrupt
14	--	--	--	Reserved
15	DMA	DMA_INTR	Rising edge	DMA controller, DMA transfer complete

Table 3: IRQ Interrupts

FIQ #	BLOCK SOURCE	SIGNAL	DEFAULT	COMMENT
0	Watchdog		Rising edge	Watchdog 0 – timer has expired
1	APB_Bus		Rising edge	Access to non-existing address on the APB
2	Multilayer_AHB		Rising edge	Access to non-existing address on the AHB
3	PLL Stat Register in SCRB		Rising edge	Group interrupt of: - I/O QVZ (EMIF: memory controller) - PLL loss state - PLL lock state See system control register PLL_STAT_REG
4	ARM processor	COMMRX	Rising edge	Interrupt for comm channel (receive)
5	ARM processor	COMMTX	Rising edge	Interrupt for comm channel (transmit)
6	Optional	Optional IRQ[15:0]	Rising edge	User-programmable IRQ source
7	Optional	Optional IRQ[15:0]	Rising edge	User-programmable IRQ source

Table 4: FIQ Interrupts

2.1.8 External Memory Interface (EMIF)

SDRAMs, SRAMs, and any I/O blocks can be connected to the external memory interface. In total, 5 chip-select lines are available:

- 1 CS line for SDRAM with 16/32-bit data width
- 4 CS lines for asynchronous memory and I/O with 8/16/32-bit data width and assignable timing

The EB 200 has a socketed boot Flash to enable a simple firmware update in stand-alone mode. The boot medium is always expected on chip select signal **CS_PER0_N**. The socketed boot Flash is addressed with CS_PER0_N by means of boot jumper J2 = "External ROM 8-bit data width" (see Section 8). The 4-Mbyte firmware Flash is then selected with CS_PER1_N. If the EB 200 is operated with a debugger (ICE), the boot Flash can be omitted as the firmware Flash can be programmed directly. The following blocks of the EB 200 can be selected with the chip-select lines:

Chip Select	I/O	Function	
		Flash-Boot 8 Bit	Flash-Boot 16 Bit
CS_PER0_N	Boot Flash / FLASH	512 Kbytes (8-bit) fixed wait states	4 Mbytes (16-bit) fixed wait states
CS_PER1_N	FLASH / SRAM	4 Mbytes (16-bit) fixed wait states	8 Mbytes (32-bit) fixed wait states
CS_PER2_N	CPLD, Ethernet, external I/O	16 Mbytes (32-bit) fixed wait states	
CS_PER3_N	FPGA for accesses to the PC host system	16 Mbytes (32-bit) ready timing	
CS_SDRAM_N	SDRAM	64 Mbytes	

Table 5: CS Areas of the EB 200

The size of the chip select areas of CS_PER0_N - CS_PER3_N is defined as 16 Mbytes. The memory areas indicated above appear mirrored correspondingly often.

The SDRAM can be regarded functionally as a dual-port RAM because the LBU interface, IRT switch, and ARM946E_S all have access to the memory due to the multimaster capability of the ERTEC 200.

2.1.9 Debug and Trace Interface

The ETM macro cell of the ARM946E-S can be used as a debug and trace interface in the ERTEC 200. With this interface, the user software running on the ARM946E-S and the user data can be analyzed and traced. The ETM module is a standard module recommended by ARM on which various available debuggers can be run. If the trace interface is used, the LBU interface is not available (configuration setting "Trace On", see Section 2.1.2). If the trace interface is used, the required parameter assignment of the ETM macro cell must be performed with the debugger, so that the required pins are switched to trace functionality.

The ETM macro cell is described in documents /9/ and /10/.

2.1.10 Serial Asynchronous Interfaces

The EB 200 has an RS232 interface with a 9-pin SUB-D male connector, which is designated X7. Only the RxD and TxD signals are lead through. The interface can be deactivated using jumper X11 11/12 (SYS_CONFIG[2]) (see also Section 2.1.2).

2.1.11 General Purpose Interface (GPIO)

The GPIO interface of the ERTEC 200 consists of 45 I/O that can be divided into two groups. The GPIOs[31:0] are multiplexed with various alternative function blocks by means of the APB bus. GPIO [31,30,1,0] can be used as inputs with interrupt capability. Alternatively, the GPIOs[44:32] can be selected for the LBU interface using the configuration setting (see Section 2.1.2).

Signal Name Function 1	Alternative Function 2	Alternative Function 3	Alternative Function 4	Use (Default)
GPIO0	P1-DUPLEX_N-LED			GPIO (interrupt-capable)
GPIO1	P2-DUPLEX_N-LED			GPIO (interrupt-capable)
GPIO2	P1-SPEED_N-100LED (TX/FX)			Bus error - LED
GPIO3	P2-SPEED_N-100LED (TX/FX)			Sync error - LED
GPIO4	P1-LINK_N-LED			Link Port1 LED
GPIO5	P2-LINK_N-LED			Link Port2 LED
GPIO6	P1-RX_N-LED	P1-TX_N-LED	P1-ACTIVE_N-LED	Activity Port1 LED
GPIO7	P2-RX_N-LED	P2-TX_N-LED	P2-ACTIVE_N-LED	Activity Port2 LED
GPIO8	UART_TXD			UART (Transmit Data, O)
GPIO9	UART_RXD			UART (Receive Data, I)
GPIO10	UART_DCD_N			GPIO
GPIO11	UART_DSR_N			GPIO
GPIO12	UART_CTS_N			GPIO
GPIO13	IRTE_TRIG_TRACE_UNIT			GPIO
GPIO14	DBGACK			GPIO
GPIO15	WD_WDOUT0_N			GPIO
GPIO16	SPI1_SSPCTL0E			GPIO
GPIO17	SPI1_SSPOE			GPIO
GPIO18	SPI1_SSPRXD			SPI1 (Receive Data; I)
GPIO19	SPI1_SSPTXD			SPI1 (Transmit Data; O)
GPIO20	SPI1_SCLKOUT			SPI1 (ClkOut Master; O)

Signal Name Function 1	Alternative Function 2	Alternative Function 3	Alternative Function 4	Use (Default)
GPIO21	SPI1_SFRMOUT			GPIO
GPIO22	SPI1_SFRMIN	DBGACK		GPIO The GPIO is used as chip select for SPI-Data-Flash or SPI-EEPROM if SPI Bootmode is selected (setting see Table 2)
GPIO23	SPI_SCLKIN	IRTE_TRIG_TRACE_UNIT		IRT-SYNC Direction (O) (RS485)
GPIO24	PLL_EXT_IN_N			IRT-SYNC Input
GPIO25	TGEN_OUT1_N			IRT-SYNC Output
GPIO26	TGEN_OUT2_N			GPIO
GPIO27	TGEN_OUT3_N			GPIO
GPIO28	TGEN_OUT4_N			GPIO
GPIO29	TGEN_OUT5_N			CPLD-TDO Input
GPIO30	TGEN_OUT6_N			ETH-INT (Ethernet-Interrupt)
GPIO31	DBGREQ			EXT-INT (external Interrupt)

Table 6: GPIO [31:0] on EB 200

Signal Name Function 1 LBU Config(6,5,2) = xx0b	Alternative Function 2 PHY-Debug Config(6,5,2) = 011b	Alternative Function 3 ETM -Trace Config(6,5,2) = 101b	Alternative Function 4 Reserved Config(6,5,2) = 111b	IO Function (Reset): see Config (6,5,2))	Int. Pull-	Remarks
LBU_A16	GPIO32	GPIO32		I/B/B (GPIO:I)	up	LBU or GPIO
LBU_A17	GPIO33	GPIO33		I/B/B (GPIO:I)	up	LBU or GPIO
LBU_A18	GPIO34	GPIO34		I/B/B (GPIO:I)	up	LBU or GPIO
LBU_A19	GPIO35	GPIO35		I/B/B (GPIO:I)	up	LBU or GPIO
LBU_A20	GPIO36	GPIO36		I/B/B (GPIO:I)	up	LBU or GPIO
LBU_SEG_0	GPIO37	GPIO37		I/B/B (GPIO:I)	up	LBU or GPIO
LBU_SEG_1	GPIO38	GPIO38		I/B/B (GPIO:I)	up	LBU or GPIO
LBU_CS_R_N	GPIO39	GPIO39		I/B/B (GPIO:I)	up	LBU or GPIO <u>LBU-Mode:</u> Chip select for accesses to paging configuration register
LBU_CS_M_N	GPIO40	GPIO40		I/B/B (GPIO:I)	up	LBU oder GPIO <u>LBU-Mode:</u> Chip Select für ERTEC200-Resourcen
LBU_D15	GPIO41	GPIO41		B/B/B (GPIO:I)	up	LBU or GPIO
LBU_RDY_N	GPIO42	GPIO42		O/B/B (GPIO:I)	up	LBU or GPIO <u>LBU-Mode:</u> LBU Ready signal: Polarity dependent on input pin LBU_POL_RDY; Output (driver always enabled);
LBU_IRQ0_N	GPIO43	GPIO43		O/B/B (GPIO:I)	up	LBU or GPIO <u>LBU-Mode:</u> Low active interrupt; No open drain
LBU_IRQ1_N	GPIO44	GPIO44		O/B/B (GPIO:I)	up	LBU or GPIO <u>LBU-Mode:</u> Low active interrupt; No open drain

Table 7: GPIO [44:32] on EB 200 as Alternative Function

Signal description: **I:** Input **O:** Output **B:** Bidirectional **P:** Power supply
Up: Internal pull-up **Dn:** Internal pull-down **(I):** Status during reset
_N at end of signal name means: Signal is **Low active** Example: **LBU_IRQ0_N**

Example of IO Function: **B/O/O/I (I) → Function 1 = Bidirectional, Function 2 = Output, Function 3 = Output, Function 4 = Input, (I) = IO Function during RESET = Input**

Note: The GPIO[44:32] are only available as Inputs on EB200, if alternative function 2 or 3 is selected.

2.2 Memory on EB 200

The following memory types are available on the EB 200 evaluation board:

2.2.1 SDRAM Interface

The SDRAM interface consists of 2 Infineon type HYP39S25616DT-7.5 blocks.

- 64-Mbyte memory capacity
- 32-bit data width
- 50 MHz clock frequency

2.2.2 SRAM Interface

The SDRAM interface consists of 2 Samsung type KF3216U6M-EF700000 blocks.

- 8-Mbyte memory capacity
- 32-bit data width

2.2.3 Flash Interface

Two different Flash types are used for the Flash interface:

1. **Socketed boot Flash**
 - AMD type AM29LV040B-90JC
 - 512-Kbyte memory capacity
 - 8-bit data width
 - Firmware can be loaded via programmer
 - No host interface required to load firmware
2. **Boot/user Flash**
 - AMD type AMD29DL323GB-90EI/T
 - 4-Mbyte memory capacity
 - 16-bit data width
 - Programming performed with JTAG
 - Intended for applications that work directly from the Flash

2.2.4 Serial Flash/EEPROM

The ERTEC 200 supports the following types in "Boot from SPI boot" mode:

- Serial data Flash, 128 Kbytes ATMEL type AT45DB011
- Serial EEPROM, 64 Kbytes ATMEL type AT25HP512

The following jumper settings are necessary:

- SPI block type (see description X11/5,6 in Section 2.1.2).
- SPI boot (see description X10 in Section 2.1.3).

GPIO[22] and GPIO[23] are used by the boot software for the SPI boot. The chip select of the SPI blocks is activated with GPIO[22], and the SPI boot mode is selected with GPIO[23].

2.3 CPLD Interface

One Lattice type LC4256C CPLD is integrated on the EB 200. The following functions are implemented with these CPLD:

- Serial memory block control, boot/normal operation
- Connection and selection of boot configuration
- Connection and selection of system configuration
- Generation of the different boot chip selects
- Forwarding of Ethernet controller interrupts
- Ready adaptation for external LAN interface
- Hardware revision level

The CPLD can be programmed with the JTAG interface X63 (for description, refer to Section 7.11).

2.4 Reset System of the EB 200

The reset system of the EB 200 has 3 reset paths:

- **Power On Reset:**
This reset is generated during power up and with the integrated reset button on the EB 200. The RESET_N signal affects the following function units.
 - Resetting of ERTEC 200 logic except for the PCI/LBU side
 - Output PHY_RES_N is activated → Discrete PHYs are reset
 - Output SRST_N is activated → Debug logic is reset
 - Output RESET_N is wired to I/O slot
- **Host – Reset:**
If the EB 200 is operated with an active host, the connected host reset acts the same as the RESET_N signal. The effects of the host reset are the same as for the power-on reset.
- **Resetting the Debug Interface:**
The debug interface is linked to the two reset signals SRST_N and TRST_N of the EB 200. This enables the debugger to initiate and monitor the reset of the following function groups.
 - Resetting of ERTEC 200 logic except for the host side (LBU interface)
 - Output PHY_RES_N is activated → Discrete PHYs are reset

The hardware reset remains active for at least 20 ms following power up.

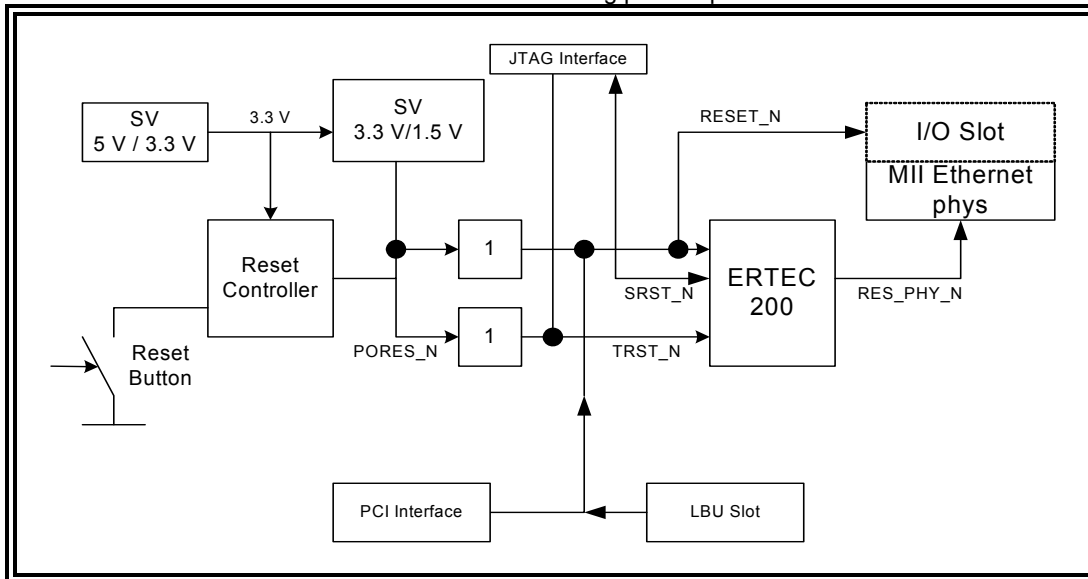


Figure 3: Reset Logic of the EB 200

2.4.1 Reset Button

The EB 200 has a reset button that initiates a manual reset of the EB 200 without disconnecting the voltage supply.

2.4.2 PCI Reset

During PCI mode, the host reset controls the evaluation board directly.

2.4.3 Watchdog and Software Reset

Additional reset events can be initiated by the watchdog or a software reset. Both reset events have the same effect as a debug reset.

2.5 Clock System of the EB 200

2.5.1 Clock-Pulse Supply of PCI Interface

The PCI bus supplies the PCI interface of the EB 200 with 33 MHz.

2.5.2 Clock Pulse Supply of EB 200 via a Quartz Crystal

By default, a 25 MHz quartz crystal supplies the EB 200 via the ERTEC 200 pins CLKP_A and CLKP_B.

2.5.3 Clock Pulse Supply of EB 200 via an Oscillator

Optionally, the EB 200 can also be supplied with an oscillator clock pulse. In this case, the 25 MHz clock pulse is feed at the ERTEC 200 pin CLKP_A.

In both cases, the available 25 MHz clock pulse generated in the ERTEC 200 via the clock pulse output REF_CLK can be used by external PHYs. The following clock pulses are generated by an internal PLL.

- Operational clock for ARM946E-S, 50/100/150 MHz
- Clock pulse for isochronous control, 100 MHz
- Clock pulse for SDRAM interface, 50 MHz

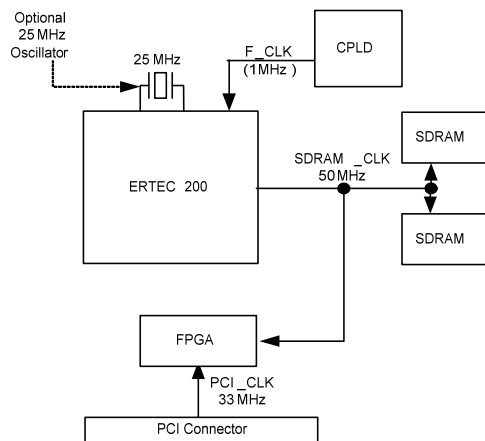


Figure 4: Overview of Clock System of the EB 200

2.5.4 Cycle for F-Timer

On the EB 200, a separate 1 MHz clock pulse is generated for the F-timer via a CPLD.

2.6 Ethernet Interface of the EB 200

The EB 200 Ethernet interface is implemented as a double electrical interface (Tx).

The PHYs have the following functionality:

- Transfer rate 100 Mbits
- Full duplex
- MDI/ MDI-X autocrossover
- Autopolarity
- Link and Activity LED functionality

After reset of the EB 200, the PHYs are inactive and must first be activated via the software. The PHYs are connected to two RJ45 Ethernet sockets via a transformer. Two LEDs for Link and Activity displays are integrated for each RJ45 socket.

3 Memory Allocation of EB 200

This section describes the address space of the EB 200 from the standpoint of the four AHB masters. The table below shows the possible accesses of the master to the slaves.

AHB Master-Slave Coupling					
Slave Master	APB Slave 1	EMIF Slave 2	DMA Slave 3	IRT Slave 4	INT Control Slave 5
ARM	X	X	X	X	X
IRT		X			
DMA	X	X			
LBU	X	X		X	

Table 8: Overview of AHB Master-Slave Access

3.1 Memory Mapping

The four AHB masters of the ERTEC 200 use the memory area differently. The table below shows the memory segments used:

Start and End Address	Seg.	Function Area for ARM9	Function Area for IRTE	Function Area for LBU	Function Area for DMA
0000 0000	0	Boot ROM(0-8 KB) EMIF-SDRAM (0-128 MB) EMIF memory (0-64 MB) D-TCM (4 KB) locked l-cache(2/4/6 KB)	Boot ROM(0-8 KB) EMIF-SDRAM (0-128 MB) EMIF memory (0-64 MB)	Boot ROM(0-8 KB) EMIF-SDRAM (0-128 MB) EMIF memory (0-64 MB)	Boot ROM(0-8 KB) EMIF-SDRAM (0-128 MB) EMIF memory (0-64 MB)
0FFF FFFF					
1000 0000	1	IRT switch controller	IRT switch controller	IRT switch controller	Not used
1FFF FFFF					
2000 0000	2	EMIF (SDRAM)	EMIF (SDRAM)	EMIF (SDRAM)	EMIF (SDRAM)
2FFF FFFF					
3000 0000	3	EMIF (Area: Bank 0-3)	EMIF (Area: Bank 0-3)	EMIF (Area: Bank 0-3)	EMIF (Area: Bank 0-3)
3FFF FFFF					
4000 0000	4	All APB macros incl. boot ROM	Not used	All APB macros incl. boot ROM	All APB macros incl. boot ROM
4FFF FFFF					
5000 0000	5	ARM-ICU	Not used	Not used	Not used
5FFF FFFF					
6000 0000	6	Not used	Not used	Not used	Not used
6FFF FFFF					
7000 0000	7	EMIF register	Not used	EMIF register	Not used
7FFF FFFF					
8000 0000	8	DMA	Not used	Not used	Not used
8FFF FFFF					
9000 0000	9 - 15	Not used	Not used	Not used	Not used
FFFF FFFF					

Table 9: Function Groups with Memory Segments Used

The D-TCM with a maximum size of 4 Kbytes can be displayed on any aligned address area. The ARM946E-S then accesses the D-TCM under this address and not the AHB bus. In addition, the locked I-cache of 2/4/6 Kbytes can be displayed on any aligned address area. Only the ARM946E-S can access both address areas.

IRT accesses to the KRAM do not use the AHB bus. These accesses are implemented in the IRT switch controller. The KRAM can be addressed starting from the memory area 0x1010_0000. An access in the non-permissible register area is detected by an IRT-internal error signal and not by an AHB acknowledgement time-out error.

3.2 Detailed Memory Description

The table below presents a detailed description of the memory segments. Mirrored segments should not be used for addressing to ensure compatible memory expansion at a later date.

Segment	Contents	Size	Address Area	Description
0	Boot ROM (0 - 8 Kbytes) or EMIF SDRAM (0-128 Mbytes) or EMIF memory (0-64 Mbytes) or Locked I-cache (2/4/6 Kbytes)	256 Mbytes	0000_0000 - 0FFF_FFFF	After reset: Boot ROM (8 Kbytes, physical; Memory swap=00b); After memory swap: EMIFSDRAM (128 Mbytes, physical; Memory swap=01b); or EMIF memory (64 Mbytes physical; Memory swap=10b); From ARM9 perspective, the locked I-cache (2/4/6 Kbytes) or a D-TCM (4 Kbytes) can be displayed.
1	IRT switch	256 Mbytes	1000_0000 - 1FFF_FFFF	2 Mbytes, physical; 2 ⁷ * mirrored; - 0-1 Mbytes for IRT register - 1-2 Mbytes for KRAM
2	EMIF (SDRAM)	256 Mbytes	2000_0000 - 2FFF_FFFF	64 Mbytes are mirrored
3	EMIF I/O Bank 0	16 Mbytes	3000_0000 - 30FF_FFFF	see Table 5
	EMIF I/O Bank 1	16 Mbytes	3100_0000 - 31FF_FFFF	see Table 5
	EMIF I/O Bank 2	4 Mbytes	3200_0000 - 323F_FFFF	CPLD (register)
	EMIF I/O Bank 2	2 Mbytes	3240_0000 - 325F_FFFF	Ethernetcontroller SMSC91C111 register
	EMIF I/O Bank 2	2 Mbytes	3260_0000 - 327F_FFFF	Ethernetcontroller SMSC91C111 data buffer
	EMIF I/O Bank 2	8 Mbytes	3280_0000 - 32FF_FFFF	external periphery and memory expansion
	EMIF I/O Bank 3	16 Mbytes	3300_0000 - 33FF_FFFF	When a smaller device is interfaced, mirroring over the entire 16 Mbytes
	Not used		3400_0000 - 3FFF_FFFF	
4	Internal boot ROM	8 Kbytes	4000_0000-4000_1FFF	8 Kbytes, physical

Segment	Contents	Size	Address Area	Description
	Timer 0 - 2	256 bytes	4000_2000 - 4000_20FF	32 bytes, physical;
	Watchdog	256 bytes	4000_2100 - 4000_21FF	28 bytes, physical;
	SPI	256 bytes	4000_2200 - 4000_22FF	256 bytes, physical;
	UART1	256 bytes	4000_2300 - 4000_23FF	256 bytes, physical;
	Not used	256 bytes	4000_2400 - 4000_24FF	256 bytes, physical;
	GPIO	256 bytes	4000_2500 - 4000_25FF	32 bytes, physical
	System control register block	256 bytes	4000_2600 - 4000_26FF	164 bytes, physical System register block of ERTEC 200
	F-counter	256 bytes	4000_2700 - 4000_27FF	8 bytes, physical
	Not used		4000_2800- 4000_FFFF	
	Not used		4001_0000- 4FFF_FFFF	
5	ARM-ICU	256 Mbytes	5000_0000- 5FFF_FFFF	ARM - Interrupt controller 128 bytes, physical
6	Not used	256 Mbytes	6000_0000- 6FFF_FFFF	
7	EMIF register	256 Mbytes	7000_0000- 7FFF_FFFF	Control register for external memory interface 64 bytes, physical
8	DMA register	256 Mbytes	8000_0000- FFFF_FFFF	DMA controller 16 bytes, physical
9 - 15	Not used	1.75 Gbyte	9000_0000- FFFF_FFFF	

Table 10: Detailed Memory Segment Distribution in the EB 200

Refer to document /2/ for a detailed description of the I/O registers for segments 4 to 8.

4 Operating Modes of the EB 200

The EB 200 is operated in stand-alone mode. An external plug-in power supply on connector is used to supply the module with regulated voltage of 6 to 9 V/1.5 A.

4.1 Operating the EB 200 without programmed Flash

This mode is used, for example, when the EB 200 evaluation board is operated with a debugger. When the EB 200 is switched on, the debugger assumes control of the EB 200. The user then assigns parameters to the required registers and loads the user software with the debug tool.

4.2 Operating the EB 200 with programmed Flash

If the EB 200 contains a programmed Flash, the boot software that is launched when the EB 200 powers up recognizes this with an entered Flash image. The boot software then branches immediately to the user software contained in the Flash. Debugging is then possible using the serial RS232 interface or the debug Ethernet port.

4.3 Operating the EB 200 with LBU Mode

If the EB 200 is operated in LBU mode, the user must take the following precautions:

- Provision of a HW reset from the host
- Provision of the 5 V voltage supply and sufficient chassis ground between the EB 200 and host
- Configuration of the EB 200 for LBU mode on connector X11 (see Section 2.1.2)
- Configuration of the selected boot mode on connector X11 (see Section 2.1.2)

If LBU boot is used as the boot mode, a local Flash does not have to be programmed because the power-up can be controlled by the host.

5 JTAG Interface

Several functions of the module can be performed with the JTAG interface of the EB 200.

- Debugging of the EB 200 on connector X61 (see circuit 1)
- Boundary scan of all boundary scan-capable ICs on connector X61 (see circuit 1)

The debugging or boundary scan selection is specified with the ERTEC 200 input TAP_SEL.

- TAP_SEL = High → BS disable → Debugging selected.
- TAP_SEL = Low → BS enable → Boundary scan selected.

In addition to debugging the EB 200, the integrated trace function of the ERTEC 200 can be used.

Various connectors are available for this purpose:

- X61 20-pin male connector according to stipulations of the ARM ETM9 macro cell for debug functionality
- X60 38-pin micro connector for debug and trace functions

The following settings are required on connector X10 and X11.

- The ETM9 module must be enabled CONFIG[6,5,2] = 101 b (see Section 2.1.2).
- Pin EN_TRACE_GPIO_N = High with SYS_CONFIG[1:0] = 01 b (see Section 2.1.2)
→ This separates the trace port from the remaining logic by means of bus switches D4 and D5.

The following companies have debuggers and trace modules for the ARM946E in their program:

- Lauterbach (JTAG Debugger/Power Trace for ARM9)
- Hitex (Tanto for ARM, Tanto Trace Port)
- ARM (RealView ICE/Debugger)
- etc.

For a description of the ETM 9 Macro Cell, see /6/.

For a description of Multi ICE, see /7/.

For a description of the IEEE Standard Test and Boundary Scan, see /8/.

Note: On X61 (JTAG-Interface) DBGRQ (Pin17) and DBGACK (Pin19) are default not used (see 7.9). The Signal „DBGACK“ is not connected to X61 Pin19. Wrongly the Signal „ETMEXTIN1“ is connected to X61 Pin19. If you need the DBGACK functionality you must change the signal connection on your EB200.

6 Settings on the EB 200

This section describes different register groups and the parameters of the CPLDs that are specified by default on the EB 200.

6.1 Default Settings of the EMIF Interface

The following settings are made on the registers of the **External Memory Interface**. The ERTEC 200 registers are described in document /2/.

Register	Address	Date	Comment
Async wait cycle config	0x7000_0004	0x4000_0080	RDY_PER_N = 1; Max_Ext_Wait = 128 (0x80) x 16 = 2048 AHB cycles
SDRAM Bank Config	0x7000_0008	0x0000_0521	9CAS, 13RAS, 2CAS Delay
SDRAM Refresh Control	0x7000_000C	0x0000_0320	Refresh every 8 us
ASYNCR Bank0 Config	0x7000_0010	0x0462_2311	16-bit, 120 ns RD&WR, 20 ns setup &hold
ASYNCR Bank1 Config	0x7000_0014	0x0462_2311	16-bit, 120 ns RD&WR, 20 ns setup &hold
ASYNCR Bank2 Config	0x7000_0018	0x0462_2312	32-bit, 120 ns RD&WR, 20 ns setup &hold
ASYNCR Bank3 Config	0x7000_001C	0x0462_2312	32-bit, 120 ns RD&WR, 20 ns setup &hold
Extended Config	0x7000_0020	0x0303_0000	Default value

Table 11: Default Settings of EMIF Registers on the EB 200

7 Connectors of the EB 200

The following connectors are available on the EB 200 for the interface connection to external components and systems.

○ PCI Interface	(X1	124-pin PCB direct connector)
○ External DC power supply	(X2	Mini-DC power jack 3.5/1.3 mm)
○ 2 Ethernet downlink interface	(X3,4	RJ45 socket with integrated magnetics + LEDs)
○ Reserved	(X6	3-pin Minitec connector)
○ UART	(X7	9-pin SubD connector)
○ GPIO [15 to 0]	(X20	2x10-pin plug connector)
○ GPIO [31 to .16]	(X21	2x10-pin plug connector)
○ GPIO [44 to .32]	(X22	2x8-pin plug connector)
○ I/O bus	(X30-32	each with 2x13-pin plug connector)
○ Trace connector for ETM of ARM946E-S	(X60	38-pin Mictor connector)
○ JTAG connectors for ICE or debugger	(X61	2x10-pin plug connector)
○ Reserved	(X62	2x5-pin plug connector)
○ Reserved	(X63	1x8-pin plug connector)

The following figure is a schematic representation of the connectors and jumper connectors, intended to help the user quickly find the required interfaces

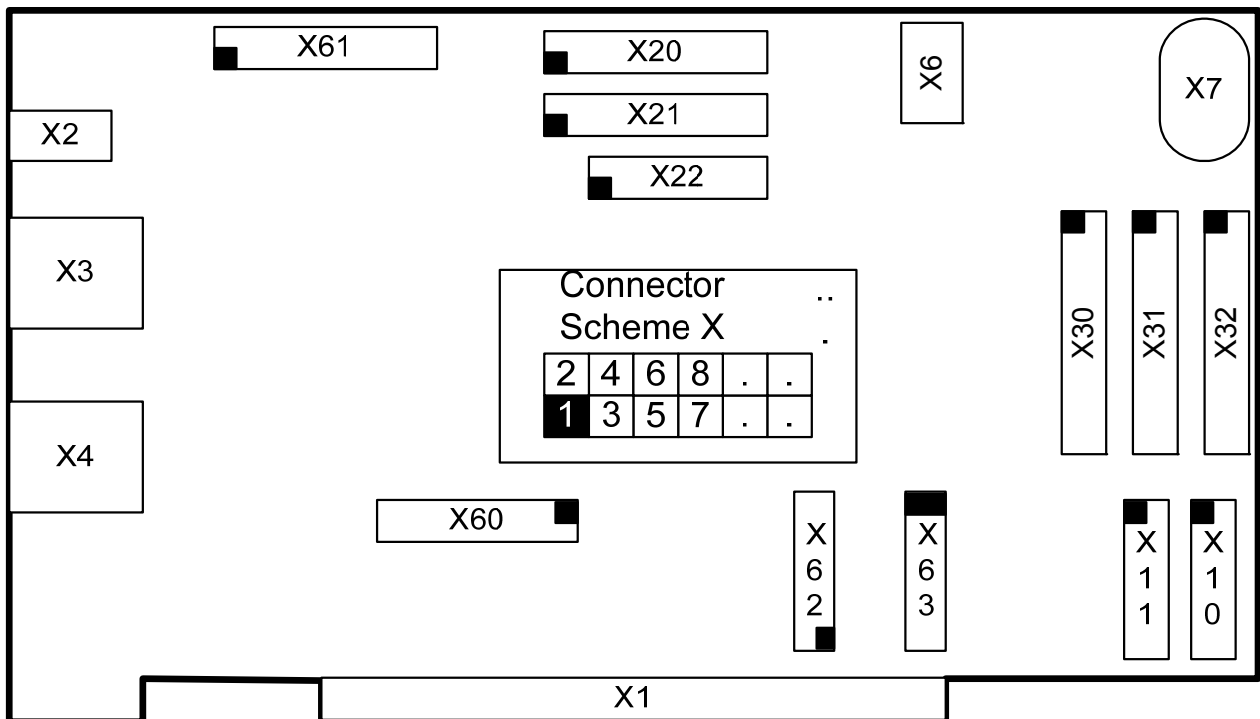


Figure 5: Connector Positions on the EB 200

7.1 PCI Interface

The PCI interface corresponds to the standardized PCI interface. The PCB direct connector has the 5V universal card characteristic. The PCI interface is used only for the function test of the EB 200.

Connector name: **X1**

Connector type: **124-pin PCB direct connector**

Pin No.	Name	Function	Pin No.	Name	Function
B1	-12 V	Supply	A1	TRST_N	JTAG
B2	TCK	JTAG	A2	+12 V	Supply
B3	M	Ground	A3	TMS	JTAG
B4	TDO	JTAG	A4	TDI	JTAG
B5	+5 V	Supply	A5	+5 V	Supply
B6	+5 V	Supply	A6	INTA_N	Interrupt
B7	INTB_N	Interrupt	A7	INTC_N	Interrupt
B8	INTD_N	Interrupt	A8	+5 V	Supply
B9	PRSENT1_N	-	A9	-	Reserved
B10	-	Reserved	A10	+Vio	I/O supply
B11	PRSENT2_N	-	A11	-	Reserved
B12	-	Key	A12	-	Key
B13	-	Key	A13	-	Key
B14	-	Reserved	A14	3.3 Vaux	Auxiliary power
B15	M	Ground	A15	RST_N	PCI reset
B16	CLK	PCI clock	A16	+Vio	I/O supply
B17	M	Ground	A17	GNT_N	Grant to master
B18	REQ_N	Request from master	A18	M	Ground
B19	+Vio	I/O supply	A19	PME_N	Interrupt power management
B20	AD[31]	Address/data	A20	AD[30]	Address/data
B21	AD[29]	Address/data	A21	+3.3 V	Supply
B22	M	Ground	A22	AD[28]	Address/data
B23	AD[27]	Address/data	A23	AD[26]	Address/data
B24	AD[25]	Address/data	A24	M	Ground
B25	+3.3 V	Supply	A25	AD[24]	Address/data
B26	CBE_N[3]	Command/byte enable	A26	IDSEL	CS for Config
B27	AD[23]	Address/data	A27	+3.3 V	Supply
B28	M	Ground	A28	AD[22]	Address/data
B29	AD[21]	Address/data	A29	AD[20]	Address/data
B30	AD[19]	Address/data	A30	M	Ground
B31	+3.3 V	Supply	A31	AD[18]	Address/data
B32	AD[17]	Address/data	A32	AD[16]	Address/data
B33	CBE_N[2]	Command/byte enable	A33	+3.3 V	Supply
B34	M	Ground	A34	FRAME_N	PCI control
B35	IRDY_N	Initiator Ready	A35	M	Ground
B36	+3.3 V	Supply	A36	TRDY_N	Target ready
B37	DEVSEL_N	Device select	A37	M	Ground
B38	M	Ground	A38	STOP_N	Stop signal
B39	LOCK_N	Lock signal	A39	+3.3 V	Supply
B40	PERR_N	Parity error	A40	-	Reserved
B41	+3.3 V	Supply	A41	-	Reserved
B42	SERR_N	System error	A42	M	Ground
B43	+3.3 V	Supply	A43	PAR	Parity signal
B44	CBE_N[1]	Command/byte enable	A44	AD[15]	Address/data
B45	AD[14]	Address/data	A45	+3.3 V	Supply
B46	M	Ground	A46	AD[13]	Address/data
B47	AD[12]	Address/data	A47	AD[11]	Address/data
B48	AD[10]	Address/data	A48	M	Ground
B49	M	Ground	A49	AD[09]	Address/data
B50	-	Key	A50	-	Key

B51	-	Key	A51	-	Key
B52	AD[08]	Address/data	A52	CBE_N[0]	Command/byte enable
B53	AD[07]	Address/data	A53	+3.3 V	Supply
B54	+3.3 V	Supply	A54	AD[06]	Address/data
B55	AD[05]	Address/data	A55	AD[04]	Address/data
B56	AD[03]	Address/data	A56	M	Ground
B57	M	Ground	A57	AD[02]	Address/data
B58	AD[01]	Address/data	A58	AD[00]	Address/data
B59	+Vio	I/O supply	A59	+Vio	I/O supply
B60	ACK64_N	Acknlg64 from master	A60	REQ64_N	Request64 from master
B61	+5 V	Supply	A61	+5 V	Supply
B62	+5 V	Supply	A62	+5 V	Supply

Table 12: Pin Assignment for PCI Interface

Key = Milling for PCI connector

7.2 LBU Interface

Instead of the PCI interface, the PCB direct connector can also be used for the LBU interface (see jumper settings in chapter 2.1.2). In this case, the following signal assignment applies:

Connector name: **X1**

Connector type: **124-pin PCB direct connector**

Pin No.	Name	Function	Pin No.	Name	Function
B1	-12 V	Supply	A1	TRST_N	JTAG
B2	TCK	JTAG	A2	+12 V	Supply
B3	M	Ground	A3	TMS	JTAG
B4	TDO	JTAG	A4	TDI	JTAG
B5	+5 V	Supply	A5	+5 V	Supply
B6	+5 V	Supply	A6	LBU_IRQ0_N	INT0 Low active
B7	LBU_IRQ1_N	INT1 Low active	A7	-	Reserved
B8	-	Reserved	A8	+5 V	Supply
B9	-	Reserved	A9	-	Reserved
B10	-	Reserved	A10	+Vio	I/O supply
B11	-	Reserved	A11	-	Reserved
B12	-	Key	A12	-	Key
B13	-	Key	A13	-	Key
B14	-	Reserved	A14	3.3 Vaux	Auxiliary power
B15	M	Ground	A15	RST_N	PCI reset (*1)
B16	CLK	PCI Clock (*1)	A16	+Vio	I/O supply
B17	M	Ground	A17	LBU_CFG	RD/WR Control: 0: separate RD and WR line 1: LBU_WR_N for RD/WR
B18	LBU_CS_M_N	CS for ERTEC 400 memory resources	A18	M	Ground
B19	+Vio	I/O supply	A19	LBU_RDY_N	Ready signal (polarity depends on LBU_POL_RDY)
B20	LBU_CS_R_N	CS for LBU Config register	A20	LBU_SEG1	Segment address
B21	LBU_SEG0	Segment address0	A21	+3.3 V	Supply
B22	M	Ground	A22	LBU_AB20	Address bus bit 20
B23	LBU_AB19	Address bus bit 19	A23	LBU_AB18	Address bus bit 18
B24	LBU_AB17	Address bus bit 17	A24	M	Ground
B25	+3.3 V	Supply	A25	LBU_AB16	Address bus bit 16
B26	LBU_AB15	Address bus bit 15	A26	LBU_AB14	Address bus bit 14
B27	LBU_AB13	Address bus bit 13	A27	+3.3 V	Supply
B28	M	Ground	A28	LBU_AB12	Address bus bit 12
B29	LBU_AB11	Address bus bit 11	A29	LBU_AB10	Address bus bit 10
B30	LBU_AB09	Address bus bit 9	A30	M	Ground
B31	+3.3V	Supply	A31	LBU_AB08	Address bus bit 8
B32	LBU_AB07	Address bus bit 7	A32	LBU_AB06	Address bus bit 6
B33	LBU_AB05	Address bus bit 5	A33	+3.3 V	Supply
B34	M	Ground	A34	LBU_AB04	Address bus bit 4
B35	LBU_AB03	Address bus bit 3	A35	M	Ground
B36	+3.3 V	Supply	A36	LBU_AB02	Address bus bit 2
B37	LBU_AB01	Address bus bit 1	A37	M	Ground
B38	M	Ground	A38	LBU_AB00	Address bus bit 0
B39	-	Reserved	A39	+3.3 V	Supply
B40	LBU_RD_N	/Read	A40	-	Reserved
B41	+3.3 V	Supply	A41	-	Reserved
B42	LBU_POL_RDY	Polarity of LBU_RDY_N	A42	M	Ground
B43	+3.3 V	Supply	A43	LBU_WR_N	/Write
B44	LBU_BE1_N	Command/Byte1 Enable	A44	LBU_DB15	15-bit data bus
B45	LBU_DB14	14-bit data bus	A45	+3.3 V	Supply

B46	M	Ground	A46	LBU_DB13	13-bit data bus
B47	LBU_DB12	12-bit data bus	A47	LBU_DB11	11-bit data bus
B48	LBU_DB10	10-bit data bus	A48	M	Ground
B49	M	Ground	A49	LBU_DB09	9-bit data bus
B50	-	Key	A50	-	Key
B51	-	Key	A51	-	Key
B52	LBU_DB08	8-bit data bus	A52	LBU_BE0_N	Command/Byte0 Enable
B53	LBU_DB07	7-bit data bus	A53	+3.3 V	Supply
B54	+3.3 V	Supply	A54	LBU_DB06	6-bit data bus
B55	LBU_DB05	5-bit data bus	A55	LBU_DB04	4-bit data bus
B56	LBU_DB03	3-bit data bus	A56	M	Ground
B57	M	Ground	A57	LBU_DB02	2-bit data bus
B58	LBU_DB01	1-bit data bus	A58	LBU_DB00	0-bit data bus
B59	+Vio	I/O supply	A59	+Vio	I/O supply
B60	-	Reserved	A60	-	Reserved
B61	+5 V	Supply	A61	+5 V	Supply
B62	+5 V	Supply	A62	+5 V	Supply

Table 13: Pin Assignment for LBU Interface

Key = Milling for PCI connector

7.3 External DC Power Supply

In stand-alone mode, the EB 200 must be supplied with an external **regulated 6-9 VDC/1,5 A power supply** by means of a connector in the front panel.

Connector name: **X2**

Connector type: **Mini-DC power jack 3.5/1.3 mm**

Pin No.	Signal Name	Function
1	DC	Potential 6-9 V
2	M	Ground 6-9 V

Table 14: Pin Assignment for External DC Supply

7.4 Double Ethernet Switch

Two RJ45 sockets with integrated magnetics are used in EB 200. The assignment of each socket corresponds to that of a switch (downlink). The integrated magnetics support autocrossover – MDI/MDIX.

Connector name: **X3, X4**

Connector type: **RJ45 socket with integrated LEDs**

Connector assignment: **Switch (downlink)**

Pin No.	Signal Name	Function
1	RX+	Receive +
2	RX-	Receive -
3	TX+	Transmit +
4	---	4 with 5 together over 75 Ohm on C to shield ground
5	---	4 with 5 together over 75 Ohm on C to shield ground
6	TX-	Transmit -
7	---	7 with 8 together over 75 Ohm on C to shield ground
8	---	7 with 8 together over 75 Ohm on C to shield ground
Shield collar	M_EXT	Shield, permanently connected

Table 15: Pin Assignment for Ethernet Switch Interface (Downlink)

The LAN cable from/to the evaluation board must not be longer than 30m.

7.5 Serial Asynchronous Interface

The ERTEC 200 has one asynchronous serial interface. The required pins are multiplexed as alternative GPIO pins. The UART, along with the RS232 interface driver, is directly connected to a 9-pin SUB-D connector. If the UART interface is not needed, the interface can be deactivated using the jumper **SYS_CONFIG[2] = OFF**.

Connector name: **X7 (UART)**

Connector type: **9-pin SUB-D connector**

Pin	Signal Name	Type	Meaning
1	-	-	-
2	RxD	I	Receive Data
3	TxD	O	Transmit Data
4	-	-	-
5	M	V	Ground
6	-	-	-
7	-	-	-
8	-	-	-
9	-	-	-

Table 16: Pin Assignment for UART

7.6 GPIO Interface

The GPIO[44 :0] are available to the user by means of three plug connectors X20-X22. In addition, the boundary scan enable signal is also located on connector X20.

Connector name: **X20**

Connector type: **2x10-pin male connector**

Pin	Signal Name	Type	Meaning
1	P3V	V	Supply
2	GPIO[0]	S	GPIO
3	GPIO[1]	S	GPIO
4	GPIO[2]	S	GPIO
5	GPIO[3]	S	GPIO
6	GPIO[4]	S	GPIO
7	GPIO[5]	S	GPIO
8	GPIO[6]	S	GPIO
9	GPIO[7]	S	GPIO
10	GPIO[8]	S	GPIO
11	GPIO[9]	S	GPIO
12	GPIO[10]	S	GPIO
13	GPIO[11]	S	GPIO
14	GPIO[12]	S	GPIO
15	GPIO[13]	S	GPIO
16	GPIO[14]	S	GPIO
17	GPIO[15]	S	GPIO
18	M	V	Ground
19	BSCAN_EN_N	S	BSCAN_EN_N
20	M	V	Ground

Table 17: Pin Assignment for GPIO [15 to 0]

Connector name: **X21**

Connector type: **2x10-pin male connector**

Pin	Signal Name	Type	Meaning
1	P3V	V	Supply
2	GPIO[16]	S	GPIO
3	GPIO[17]	S	GPIO
4	GPIO[18]	S	GPIO
5	GPIO[19]	S	GPIO
6	GPIO[20]	S	GPIO
7	GPIO[21]	S	GPIO
8	GPIO[22]	S	GPIO
9	GPIO[23]	S	GPIO
10	GPIO[24]	S	GPIO
11	GPIO[25]	S	GPIO
12	GPIO[26]	S	GPIO
13	GPIO[27]	S	GPIO
14	OPIO[28]	S	GPIO
15	GPIO[29]	S	GPIO
16	GPIO[30]	S	GPIO
17	GPIO[31]	S	GPIO
18	M	V	Ground
19	M	V	Ground
20	M	V	Ground

Table 18: Pin Assignment for GPIO [31 to .16]

Note: The GPIO[44:32] are only available as Inputs on EB200 if Alternativfunctions 2 or 3 are selected. They are connected on X22

Connector name: **X22**

Connector type: **2x8-pin male connector**

Pin	Signal Name	Type	Meaning
1	P3V	V	Supply
2	GPIO[32]	S	GPIO
3	GPIO[33]	S	GPIO
4	GPIO[34]	S	GPIO
5	GPIO[35]	S	GPIO
6	GPIO[36]	S	GPIO
7	GPIO[37]	S	GPIO
8	GPIO[38]	S	GPIO
9	GPIO[39]	S	GPIO
10	GPIO[40]	S	GPIO
11	GPIO[41]	S	GPIO
12	GPIO[42]	S	GPIO
13	GPIO[43]	S	GPIO
14	OPIO[44]	S	GPIO
15	M	V	GPIO
16	M	V	GPIO

Table 19: Pin Assignment for GPIO [44 to 32]

7.7 I/O Adapter

The complete EMIF interface is wired to the I/O adapter connectors X30 to X32 for connecting external I/O and memory to the EB 200.

Connector name: **X30**

Connector type: **2x13-pin plug connectors**

Pin No.	Signal Name	Function
1	P3V	3.3 V
2	B AI[0]	EMIF Address Bit 0 buffered
3	B AI[1]	EMIF Address Bit 1 buffered
4	B AI[2]	EMIF Address Bit 2 buffered
5	B AI[3]	EMIF Address Bit 3 buffered
6	B AI[4]	EMIF Address Bit 4 buffered
7	B AI[5]	EMIF Address Bit 5 buffered
8	B AI[6]	EMIF Address Bit 6 buffered
9	B AI[7]	EMIF Address Bit 7 buffered
10	B AI[8]	EMIF Address Bit 8 buffered
11	B AI[9]	EMIF Address Bit 9 buffered
12	B AI[10]	EMIF Address Bit 10 buffered
13	B AI[11]	EMIF Address Bit 11 buffered
14	B AI[12]	EMIF Address Bit 12 buffered
15	B AI[13]	EMIF Address Bit 13 buffered
16	B AI[14]	EMIF Address Bit 14 buffered
17	B AI[15]	EMIF Address Bit 15 buffered
18	B AI[16]	EMIF Address Bit 16 buffered
19	B AI[17]	EMIF Address Bit 17 buffered
20	B AI[18]	EMIF Address Bit 18 buffered
21	B AI[19]	EMIF Address Bit 19 buffered
22	B AI[20]	EMIF Address Bit 20 buffered
23	B AI[21]	EMIF Address Bit 21 buffered
24	B AI[22]	EMIF Address Bit 22 buffered
25	B AI[23]	EMIF Address Bit 23 buffered
26	M	Ground

Table 20: Pin Assignment for X30 EMIF Address Bits

Connector name: **X31**

Connector type: **2x13-pin plug connectors**

Pin No.	Signal Name	Function
1	P3V	3.3 V
2	B DI[0]	EMIF data bit 0 buffered
3	B DI[1]	EMIF data bit 1 buffered
4	B DI[2]	EMIF data bit 2 buffered
5	B DI[3]	EMIF data bit 3 buffered
6	B DI[4]	EMIF data bit 4 buffered
7	B DI[5]	EMIF data bit 5 buffered
8	B DI[6]	EMIF data bit 6 buffered
9	B DI[7]	EMIF data bit 7 buffered
10	B DI[8]	EMIF data bit 8 buffered
11	B DI[9]	EMIF data bit 9 buffered
12	B DI[10]	EMIF data bit 10 buffered
13	B DI[11]	EMIF data bit 11 buffered
14	B DI[12]	EMIF data bit 12 buffered
15	B DI[13]	EMIF data bit 13 buffered
16	B DI[14]	EMIF data bit 14 buffered
17	B DI[15]	EMIF data bit 15 buffered
18	B DI[16]	EMIF data bit 16 buffered
19	B DI[17]	EMIF data bit 17 buffered
20	B DI[18]	EMIF data bit 18 buffered
21	B DI[19]	EMIF data bit 19 buffered
22	B DI[20]	EMIF data bit 20 buffered
23	B DI[21]	EMIF data bit 21 buffered
24	B DI[22]	EMIF data bit 22 buffered
25	B DI[23]	EMIF data bit 23 buffered
26	M	Ground

Table 21: Pin Assignment for X31 EMIF Data Bits

Connector name: **X32**

Connector type: **2x10-pin plug connectors**

Pin No.	Signal Name	Function
1	P3V	3.3 V
2	B DI[24]	EMIF data bit 24 buffered
3	B DI[25]	EMIF data bit 25 buffered
4	B DI[26]	EMIF data bit 26 buffered
5	B DI[27]	EMIF data bit 27 buffered
6	B DI[28]	EMIF data bit 28 buffered
7	B DI[29]	EMIF data bit 29 buffered
8	B DI[30]	EMIF data bit 30 buffered
9	B DI[31]	EMIF data bit 31 buffered
10	B BE2 N	Byte enable 2 for B DI[23:16] buffered
11	B BE3 N	Byte enable 3 for B DI[31:24] buffered
12	B BE0 N	Byte enable 0 for B DI[7:0] buffered
13	B BE1 N	Byte enable 1 for B DI[15:8] buffered
14	B RD N	EMIF read strobe buffered
15	B WR N	EMIF write strobe buffered
16	CS ETH N	Address enable Ethernet debug port
17	CS ETH D N	DATA CS Ethernet debug port (I/O adapter)
18	EXT CS N	Chip select for I/O expansion
19	EXT RDY N	Ready signal for I/O expansion
20	EXT INT N	Interrupt for I/O expansion
21	M	Ground
22	M	Ground
23	M	Ground
24	M	Ground
25	M	Ground
26	M	Ground

Table 22: Pin Assignment for Connectors of I/O Adapter

7.8 Trace Interface

For connecting a trace interface to the ETM macro cell of the ARM946E-S

Connector name: **X60**

Connector type: **38-Pin micro direct connector (optional flat ribbon cable available)**

Pin No.	Signal Name	Function
1	NC	Not Connected
2	NC	Not Connected
3	NC	Not Connected
4	NC	Not Connected
5	M	Not Connected
6	Trace clock	Clock of the trace interface
7	DBREQ	Debug Request
8	DBGACK	Default not used with test board
9	SRST_N	System Reset
10	EXTRIG	Default not used with test board
11	TDO	JTAG Test Data Out
12	VTREF	3.3 V reference voltage
13	Not used (RTCK)	Not used
14	VCC	Supply
15	TCK	JTAG test clock
16	TRACEPKT7	TRACE data bit 7
17	TMS	JTAG test mode select
18	TRACEPKT6	TRACE data bit 6
19	TDI	JTAG data in
20	TRACEPKT5	TRACE data bit 5
21	TRST_N	JTAG Reset
22	TRACEPKT4	TRACE data bit 4
23	TRACEPKT15	TRACE data bit 15 = M for test board
24	TRACEPKT3	TRACE data bit 3
25	TRACEPKT14	TRACE data bit 14 = M for test board
26	TRACEPKT2	TRACE data bit 2
27	TRACEPKT13	TRACE data bit 13 = M for test board
28	TRACEPKT1	TRACE data bit 1
29	TRACEPKT12	TRACE data bit 12 = M for test board
30	TRACEPKT0	TRACE data bit 0
31	TRACEPKT11	TRACE data bit 11 = M for test board
32	TRACESYNC	TRACESYNC
33	TRACEPKT10	TRACE data bit 10 = M for test board
34	PIPESTAT2	TRACE Pipeline Status 2
35	TRACEPKT9	TRACE data bit 9 = M for test board
36	PIPESTAT1	TRACE Pipeline Status 1
37	TRACEPKT8	TRACE data bit 8 = M for test board
38	PIPESTAT0	TRACE Pipeline Status 0

Table 23: Pin Assignment for Trace Interface

7.9 JTAG Interface

For connecting a debugger or ICE.

Connector name: **X61**

Connector type: **2x10-pin male connector**

Pin No.	Signal Name	Function
1	VTREF	3.3 V reference voltage
2	VSUPPLY	3.3 V
3	TRST_N	JTAG reset
4	M	Ground
5	TDI	JTAG data in
6	M	Ground
7	TMS	JTAG test mode select
8	M	Ground
9	TCK	JTAG test clock
10	M	Ground
11	Not used (RTCK)	Synchronous JTAG clock (not used in ERTEC 200)
12	M	Ground
13	TDO	JTAG Test Data Out
14	M	Ground
15	SRST_N	System Reset
16	M	Ground
17	Not used (DBREQ)	Default not used with test board
18	M	Ground
19	Not used (DBGACK)	Default not used with test board
20	M	Ground

Table 24: Pin Assignment of JTAG Interface

7.10 JTAG Programming Interface for FPGA (Byte Blaster)

JTAG interface for interfacing of PCI-FPGAs.

Connector name: **X62**

Connector type: **2x5-pin male connector**

Pin No.	Signal Name	Function
1	TCK	JTAG test clock
2	M	Ground
3	TDO	JTAG data out
4	VSUPPLY	3.3 V
5	TMS	JTAG test mode select
6	-	-
7	-	-
8	-	-
9	TDI	JTAG data in
10	M	Ground

Table 25: Pin Assignment for Byte Blaster FPGA Programming Interface

7.11 CPLD Programming Interface

The two PLDs on the EB 200 can be parameterized with a programming adapter. The two PLDs are connected in a daisy chain pattern.

Connector name: **X63**

Connector type: **1x8-pin plug connectors**

Pin	Signal Name	Type	Meaning
1	P3V	V	Supply
2	TDO	O	Serial data out
3	TDI	I	Serial data in
4	-	-	-
5	-	-	-
6	TMS	I	Test mode select
7	M	V	Ground
8	TCK	I	Test clock

Table 26: Pin Assignment for CPLD Programming Interface

8 Settings on the EB 200

Two connectors for various settings are integrated in the EB 200. These are used to specify various modes and selections of function groups on the EB 200:

- Selection of boot medium and boot software
- Selection of the ERTEC 200 configuration
- Activation/deactivation of different board functions

The exact position of the two connectors is shown schematically in Section 7.

The following convention applies to all connectors:

- **0 = Jumper connected**
- **1 = Jumper not connected**

8.1 Boot/Configuration Connector X10

Connector X10 is used to specify the boot modes and, in some cases, the configuration modes on the EB 200.

Connector name: **X10**

Connector type: **2x8 pin male connector**

Pin	Signal Name	Type	Meaning
1	M		
2	BOOT[0]		
3	M		
4	BOOT[1]		
5	M		
6	BOOT[2]		
7	M		
8	BOOT[3]		
9	M		
10	CONFIG[1]		
11	M		
12	CONFIG[2]		
13	M		
14	CONFIG[3]		
15	M		
16	CONFIG[4]		

Table 27: Connector X10 for Boot Settings and Some Configuration Settings

8.2 System/Configuration Connector X11

Connector X11 is used to specify the remaining configuration modes and various system functions on the EB 200 (for a description of system and configuration modes, refer to Section 2.1.2).

Connector name: **X11**

Connector type: **2x8 pin male connector**

Pin	Signal Name	Type	Meaning
1	M		
2	CONFIG[5]		
3	M		
4	CONFIG[6]		
5	M		
6	SPI_CONFIG		
7	M		
8	SYS_CONFIG[0]		
9	M		
10	SYS_CONFIG[1]		
11	M		
12	SYS_CONFIG[2]		
13	M		
14	SYS_CONFIG[3]		
15	M		
16	SYS_CONFIG[4]		

Table 28: Connector X11 for Configuration and System Settings

9 Structure of the EB 200

9.1 Mechanical Structure

The EB 200 is designed as a PC module with a 174 mm short PCI format. The EB 200 has a standard PC slot plate. The board is equipped with 4 holes onto which the supplied spacers are mounted.

9.2 Front and Display Element

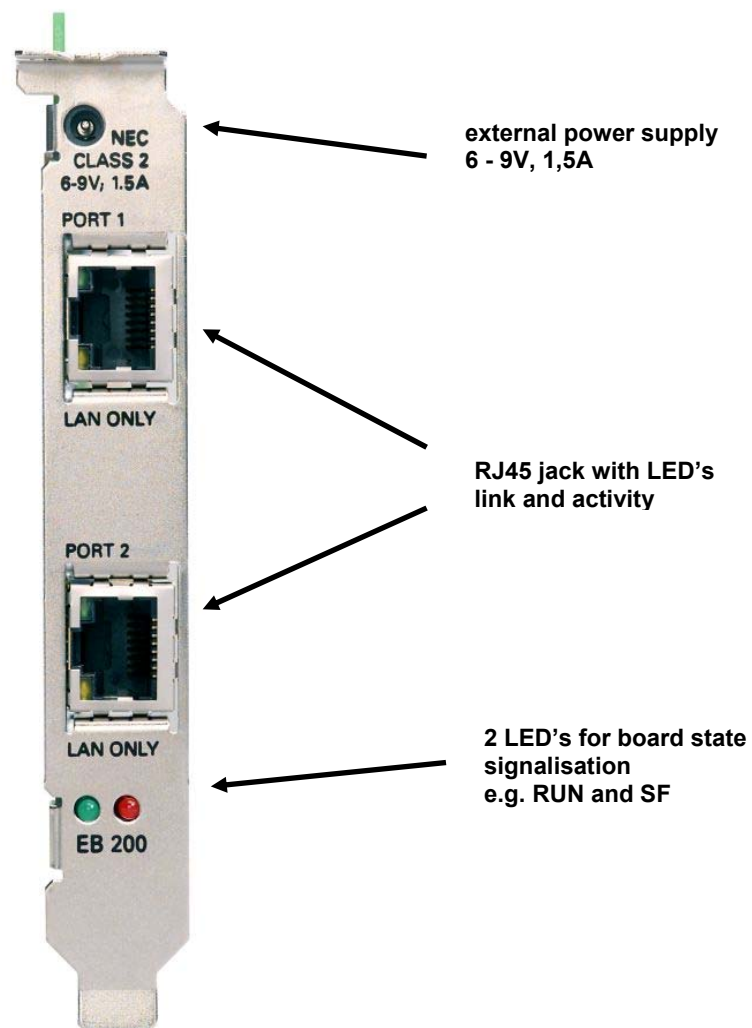


Figure 6: Front Element of the EB 200

The table below presents the display elements and their functions.

LED	Color	Function
Link Port1 (GPIO 4)	Green	On = Port 1 has link
Activity Port1 (GPIO 6)	Yellow	On (80 ms) = Message frame on Port 1 received or transmitted
Link Port2 (GPIO 5)	Green	On = Port 2 has link
Activity Port2 (GPIO 7)	Yellow	On (80 ms) = Message frame on Port 2 received or transmitted
Fault (GPIO 2)	Red	On = Bus fault of ERTEC200 starter kit
Sync (GPIO 3)	Green	On = ERTEC200 starter kit has been synchronized to the network clock

Table 29: Function of LEDs on Front Panel of the EB 200

The display LEDs of the RJ45 sockets are directly connected to the LED outputs of the PHYs integrated in the ERTEC 200. Optionally, these LED outputs can be converted to a GPIO-alternative function. In this way, software can be used to control the LED activation.

10 Miscellaneous

10.1 Acronyms/Glossary:

AHB	AMBA Advanced High Performance Bus (Multimaster, bursts)
AMBA	Advanced M icrocontroller B us A rchitecture
APB	AMBA Advanced P eripheral B us (Single master, bursts)
BF	B us fault
BIST	B uilt I n S elf T est
DTCM	D ata T ightly C oupled M emory
EB	E valuation B oard
ERTEC	E nhanced R eaL-Time E thernet C ontroller
EMIF	E xternal M emory I nterface
ETM	E mbedder T race M acrocell
GPIO	G eneral P urpose I nput/ O utput
ICU	I nterrupt C ontroller U nit
IP	I ntellectual P roperty
IRQ	I nterrupt R equest
IRT	I sochronous R eal T ime
ITCM	I nstruction T ightly C oupled M emory
JTAG	J oint T est A ction G roup
LBU	L ocal B us U nit
NMI	N on M askable I nterrupt
PLL	P hased L ocked L oop
PROFINET	P rofinet device connection via E thernet
SCRB	S ystem C ontrol R egister B lock
SDRAM	S ynchronous D ynamic R AM
SPI	S tandard S erial P eripheral I nterface
SRAM	S tatic R AM
SW	S oftware
UART	U niversal A synchronous R eceiver / T ransmitter
WS	W arteschlange (queue)

10.2 References:

- /1/ ERTEC 200 Data Sheet V1.1.1 (ERTEC200_Data Sheet_V111.PDF);
- /2/ ERTEC 200 Manual V1.1.1 (ERTEC200_Manual_V111.PDF);
- /3/ Guideline_DK_ERTEC200_400_PNIO_ECOS_V310.pdf;
- /4/ Technical Reference Manual ARM946E-S REV1 16 February 2001 (DDI 0201A_946ES.PDF);
- /5/ Technical Reference Manual ARM946E-S 16 December 1999 (DDI_0165A_9E-S_TRM. PDF);
- /6/ Embedded Trace Macrocell Architecture Specification (ETM_Spec.PDF);
- /7/ Multi-ICE System Design Consideration Applic.-Note 72 (DAI0072A_Multiicedesign-Notes.PDF);
- /8/ IEEE Standard Test Access Port and Boundary-Scan Architecture (1149.1 IEEE Boundary Scan 2001.PDF);
- /9/ ETM9 Technical Reference Manual (Rev. 2a) (ARM DDI 0157E)
- /10/ ETM Specification (ARM IHI 0014 H)